

# Test Qualification Plan

## 1. SCM Correlation Data Gathering

- Loop 4 bin1 units x30
- Run 100 bin1 units on handler
- Serialize and test 10 bin1 units
- Serialize and test 5 reject units

## 2. Ship correlation package from SCM to SCC

## 3. SCC Correlation Data Gathering

- Loop 4 bin1 units x30
- Run 100 bin1 units on handler
- Test 10 already serialized bin1
- Test 5 already serialized rejects

## 4. SCM/SCC send data to ADGT for Data Crunching and Analysis

## 5. CorL8 Analysis of x30 loop /100 units handler data

- X30 loop must pass Mean Shift, Sigma Spread and CPK criteria
- 100 Bin1 Correlation units must pass Mean Shift, Sigma Spread and CPK criteria
- 10 serialized units must pass bin1 both in SCC and in SCM
- 5 serialized rejects must fail the same parameter for both SCC and SCM

## 6. Correlation Data Approval

- For TRB movement to Available with Condition

## 7. Validation lot run handled by SCC

Note: CorL8 is ADI data analysis tool.



Reject Correlation		
Unit	SCM	SCC
1	TnumX: XXXXX	TnumX: XXXXX
...	TnumX: XXXXX	TnumX: XXXXX
5	TnumX: XXXXX	TnumX: XXXXX

Bin1 Correlation		
Unit	SCM	SCC
1	Pass	Pass
...	Pass	Pass
10	Pass	Pass

Correlation Test Criteria(TST00137)	
<b>% Mean Shift Criteria</b>	$(( \text{SCM\_mean} - \text{SCC\_Mean} ) / ( \text{Upper\_Limit} - \text{Lower\_Limit} )) \times 100 < 5$
<b>Sigma Spread Criteria</b>	$( \text{SCC\_Sigma} / \text{SCM\_Sigma} ) < 1.300000$
<b>Cpk Criteria</b>	If Cpk to the test limits is >10, then test given automatically PASS

# Test Qualification estimated Timeline

Devices	Oct, 2013 to Nov, 2013	Dec, 2013 to Apr, 2014	May, 2014
SCM Correlation Data Gathering&Shipment	PLANNED	PLANNED	
SCC Correlation Data Gathering		PLANNED	
Data Review and Approved by ADGT		PLANNED	
Validation Run/TRB Closure		PLANNED	PLANNED

 PLANNED  
 ACTUAL/ADJUSTED

# Bill of Materials

	SCM	SCC	Remarks
Die Attach	Ablestik 8290	Ablestik 8290	Same BOM
Wire type	Gold MKE UR2	Gold MKE UR2	
Mold Compound	Sumitomo G770	Sumitomo G770	
Lead Finish	Matte Sn	Matte Sn	

## Reliability Qualification Plan for LFCSP Package at STATS ChipPAC China (SCC)

QUALIFICATION PLAN			
Test	Conditions	Sample Size	Expected Completion Date
Highly Accelerated Stress Test (HAST)*	JEDEC <i>JESD22-A110</i>	<b>3 x 82</b>	April 2014
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	<b>3 x 82</b>	April 2014
Autoclave (AC)*	JEDEC <i>JESD22-A102</i>	<b>3 x 82</b>	April 2014
Solder Heat Resistance (SHR)*	<i>ADI-0049</i>	<b>3 x 11</b>	April 2014
High Temperature Storage (HTS)	JEDEC <i>JESD22-A103</i>	<b>1 x 82</b>	April 2014
Field Induced Charged Device Model (FICDM)	JEDEC <i>JESD22-C101</i>	<b>3/Voltage</b>	April 2014

\*These samples will be subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Soak: Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.